EXHIBIT B

Bounding uncertainty in the static timing analysis of digital PD-SOI circuits

(with application to static noise analysis)

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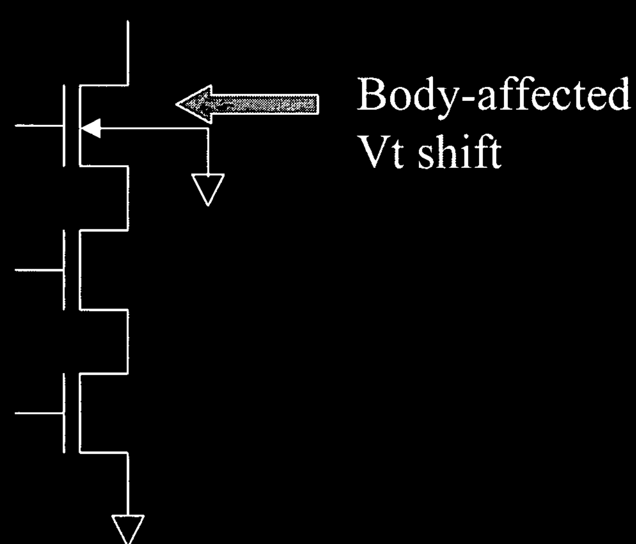
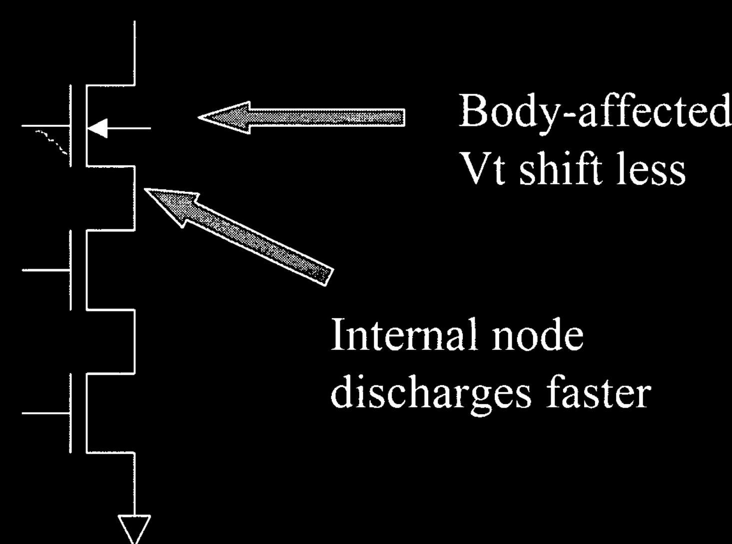
Advantages of SOI

- Reduced source/drain diffusion capacitance
- Improved stack performance
- Some reduction in wire capacitance
- Gives advantage to certain circuit families (e. g. passgates)

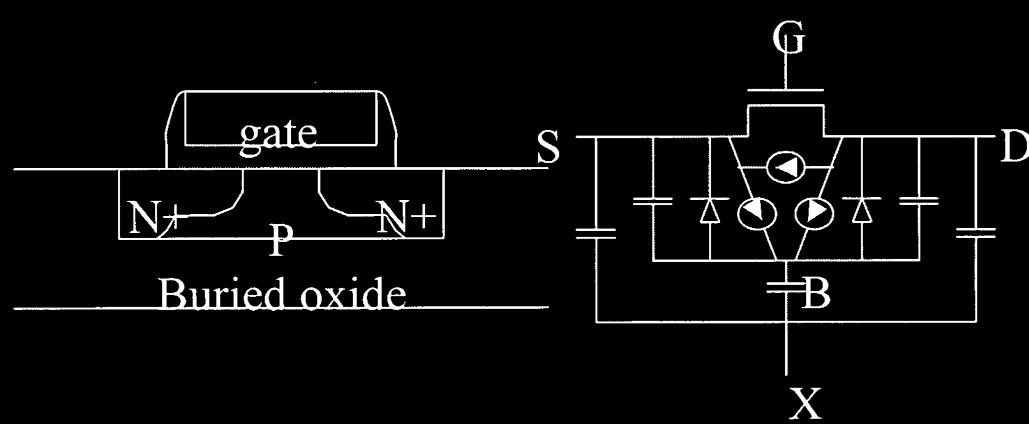




Target technology for experiments

- IBM Sematech "benchmark" technology
  - L_{drawn} = 0.35 um
  - T_{ox} = 4.5 nm
  - T_{box} = 80 nm
- Core simulation technology is spice3f5 wrapped with an API and BSIM3-SOI models. Still debugging transient analysis accuracy!

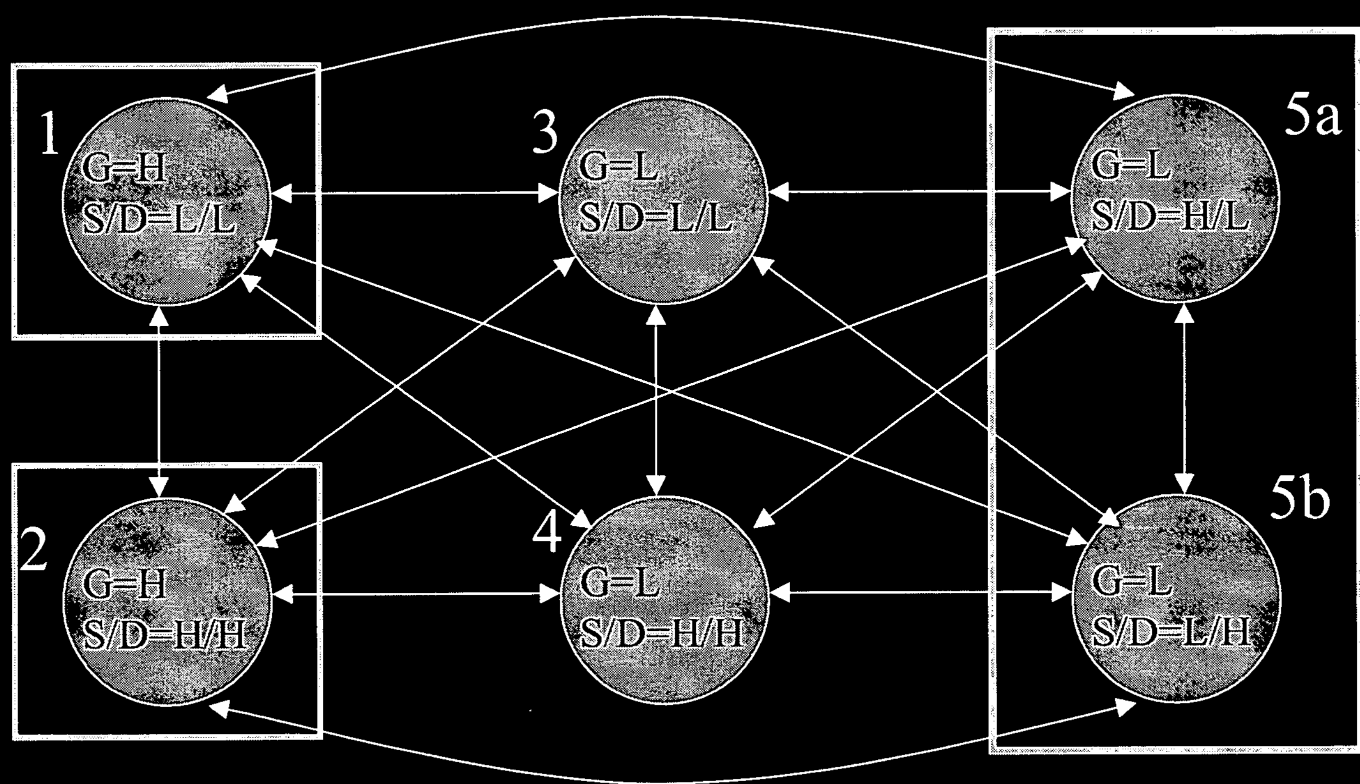
Body voltage determined by...



- Capacitive coupling of gate, substrate, source, and drain
- Forward-bias diode currents at the source-body and drain-body junctions
- Reverse-bias diode currents at the source-body and drain-body junctions

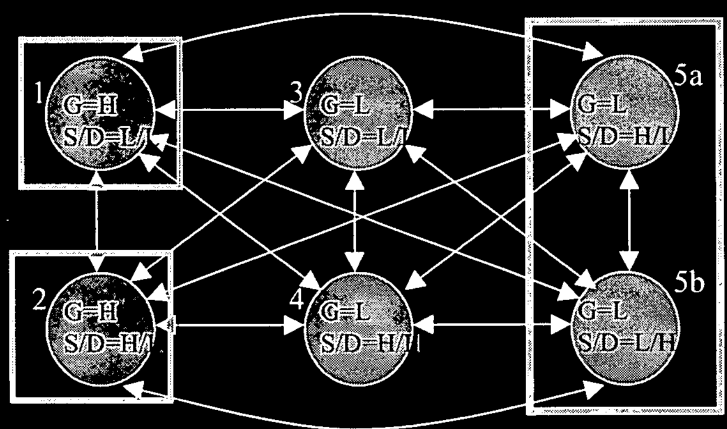
State diagram view of body interactions

nMOS



Device physics in this picture

Each state transition involves a "capacitive" coupling kick:

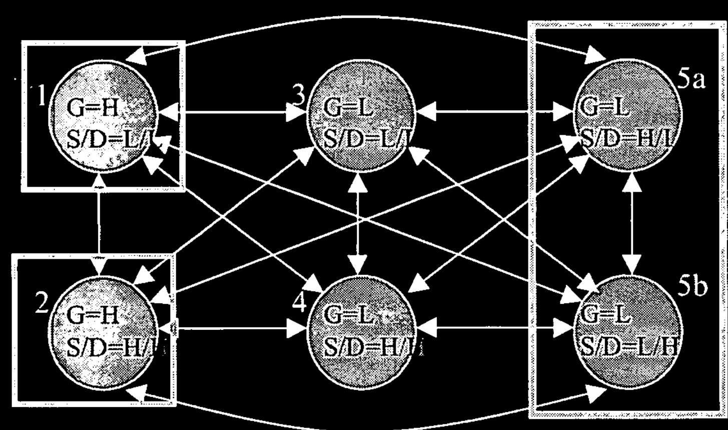


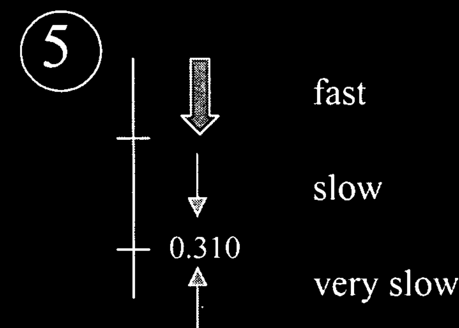
1->2	1200 mV
1->3	-300 mV
1->4	-200 mV
1->5	-200 mV
2->1	-950 mV/-1700 mV
2->3	-1300 mV/-2100 mV
2->4	-1450 mV/-950 mV
2->5	-16 mV/-1800 mV
3->1	300 mV
3->2	1650 mV
3->4	125 mV
3->5	95 mV
4->1	200mV/-1500 mV
4->2	1450 mV/950 mV
4->3	-110 mV/-1500 mV
4->5	-20 mV/-1300 mV
5->1	200 mV
5->2	1500 mV
5->3	-95 mV
5->4	20 mV

Capacitive kicks largely "reversible" except for cases of forward-bias body discharge. But are important for "initial condition" analysis.

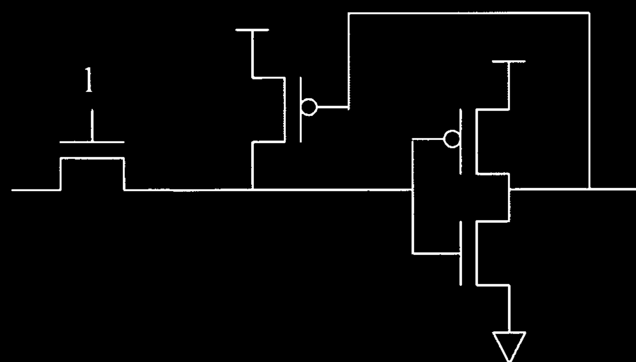
Device physics in this picture

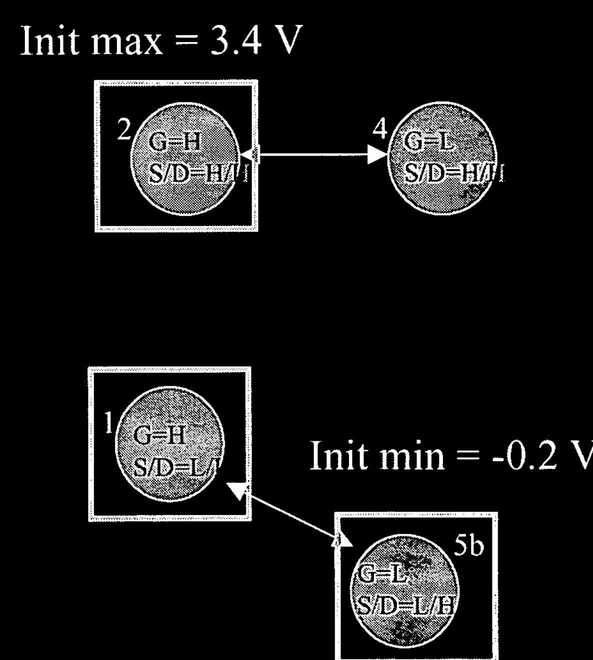
Each state has a steady-state target with relaxation time dependent on deviation from the target.

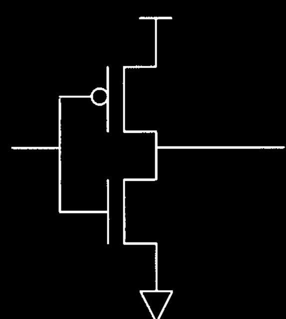




"Initial condition" analysis

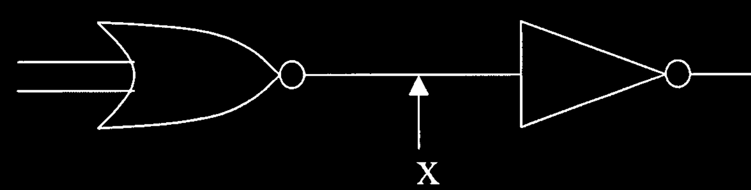


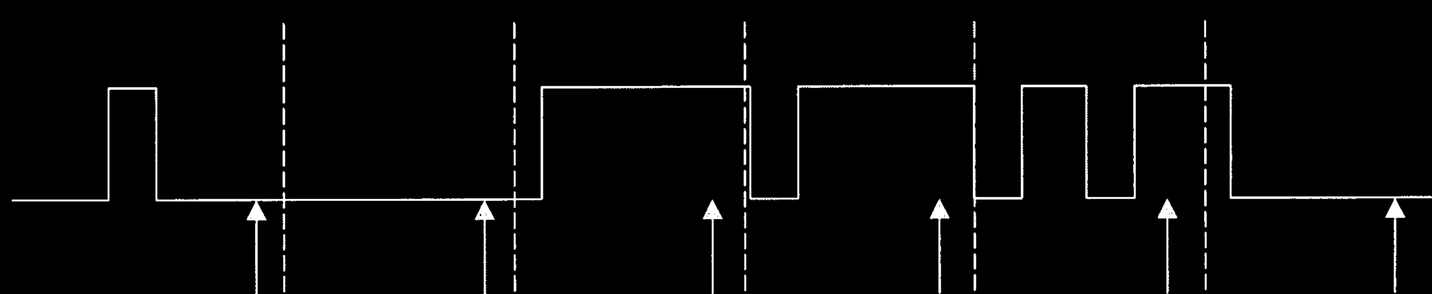




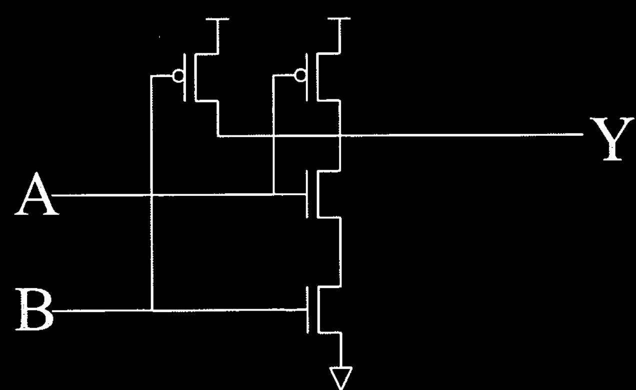
Signal Probability

$P_s(x) =$ Average fraction of clock cycles in which the steady state value of x is a logic high





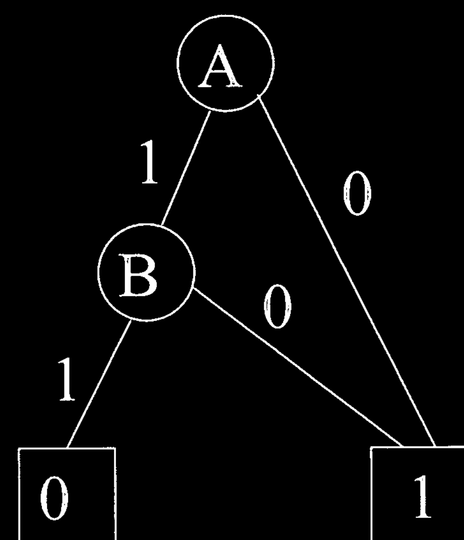
Signal Probability



$$P_s(A) = 0.5$$

$$P_s(B) = 0.5$$

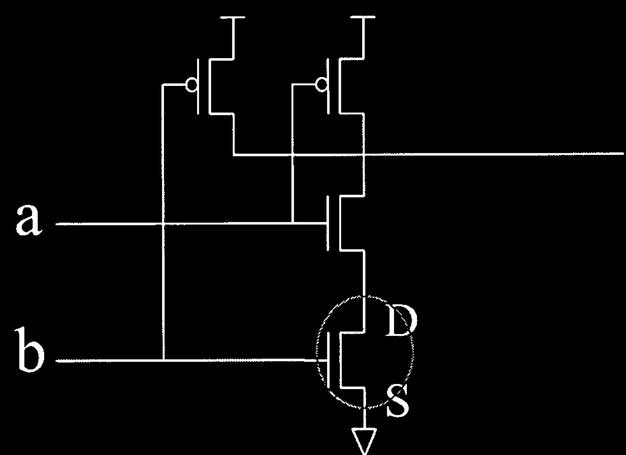
$$P_s(Y) = 1 - P_s(A)P_s(B) = 0.75$$



Easily done with BDD techniques

P(^A) + P(A)P(^B)

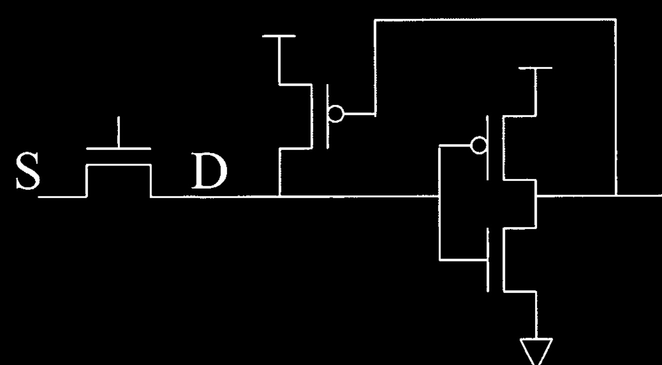
Conditional channel switching probabilities



Do NOT sum to 1

P(D|^b) = P(a)
P(^D|^b) = 0
P(S|b) = 0
P(^S|b) = 1

P(S|^b) = 0
P(^S|^b) = 1

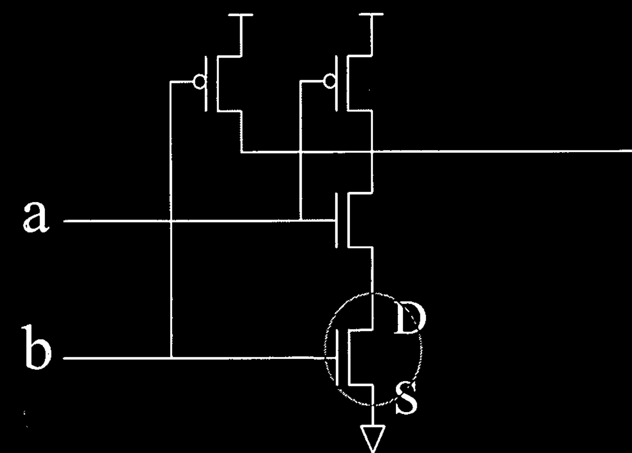


P(S|G) = 0.5
P(^S|G) = 0.5
P(^S|^G) = 0.5
P(S|^G) = 0.5

P(D|^G) = 0
P(^D|^G) = 0

Done through a path search assuming both temporal and spatial independence of CCC input variables.

Hazards



a

R max/min = 200/800
F max/min = 200/800

b

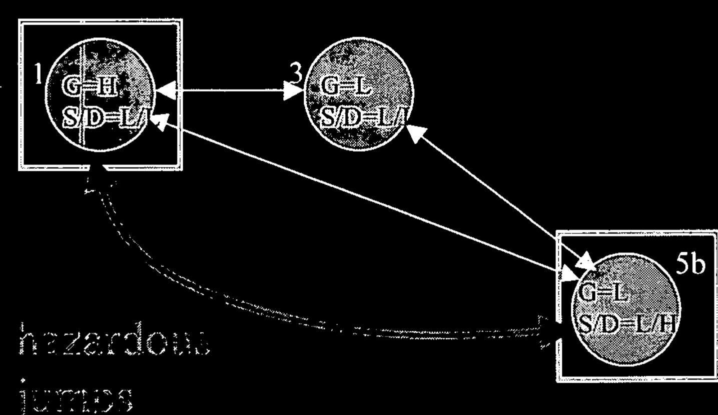
R max/min = 400/600
F max/min = 400/600

b = H

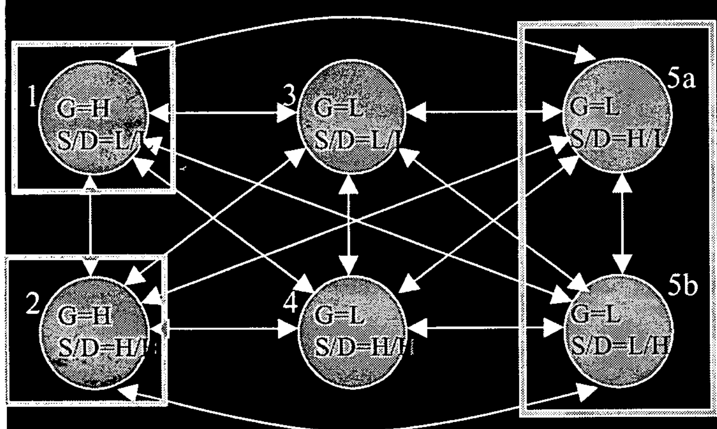
D F max = 600
D F min = 400
D R max = NA
D R min = NA

b = L

D R max = 800
D R min = 200
D F max = NA
D R min = NA



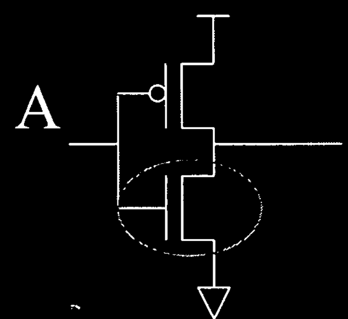
Monte Carlo analysis



Inputs
- signal probability of gate
- channel conditional probabilities on gate disposition
- channel conditional hazard R/F times on gate disposition

Process (done separately for min and max)
- use first two cycles to establish initial condition
- then use probabilities:
  - assign next gate using signal probability
  - given next gate assignment, find S/D assignment
  - given current state and next state, affect transition to achieve min/max result, allowing hazards

Monte Carlo results

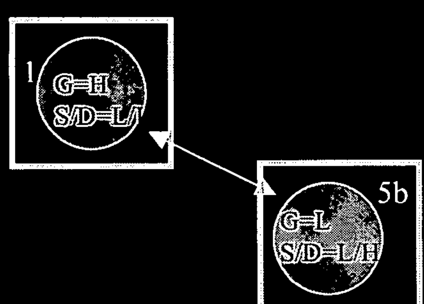


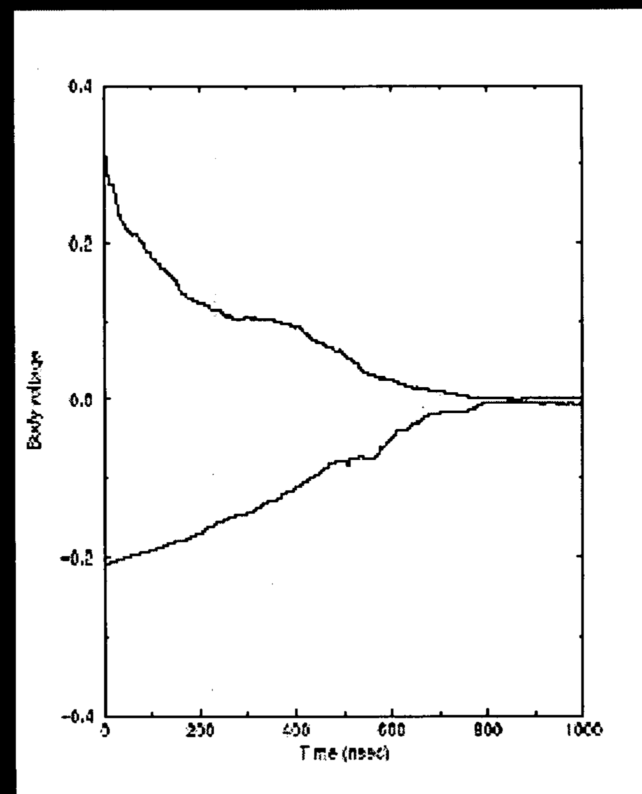
G/S/D = L/L/H

P(A) = 0.5

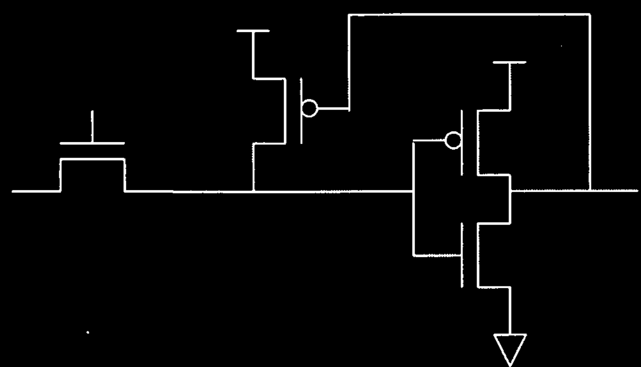
T_{cycle} = 1000 psec

R/F min/max = 400 ps / 600 ps





Monte Carlo results (con't)

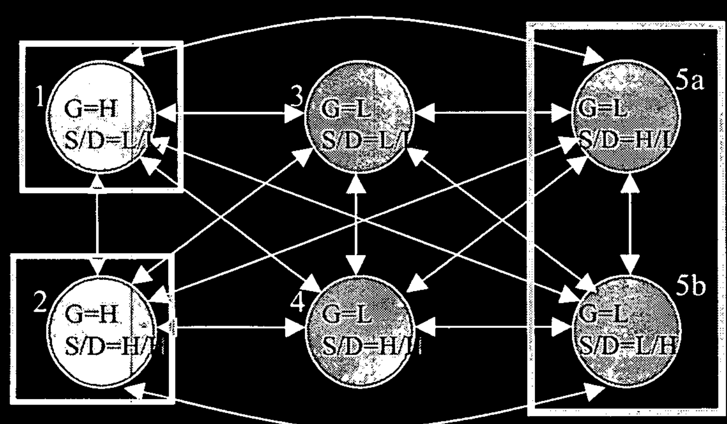


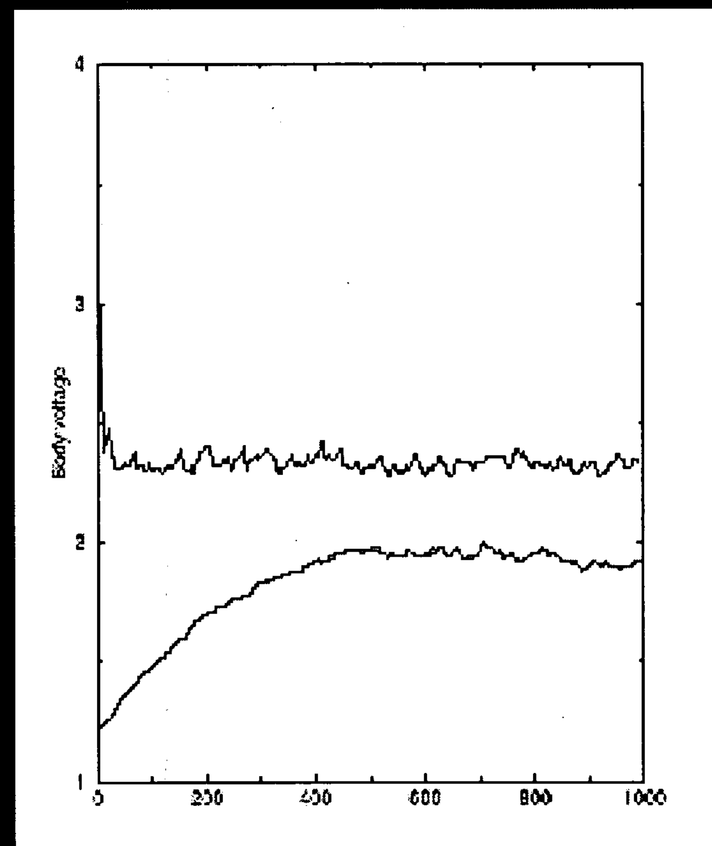
G/S/D = H/H/H

All probabilities are 0.5

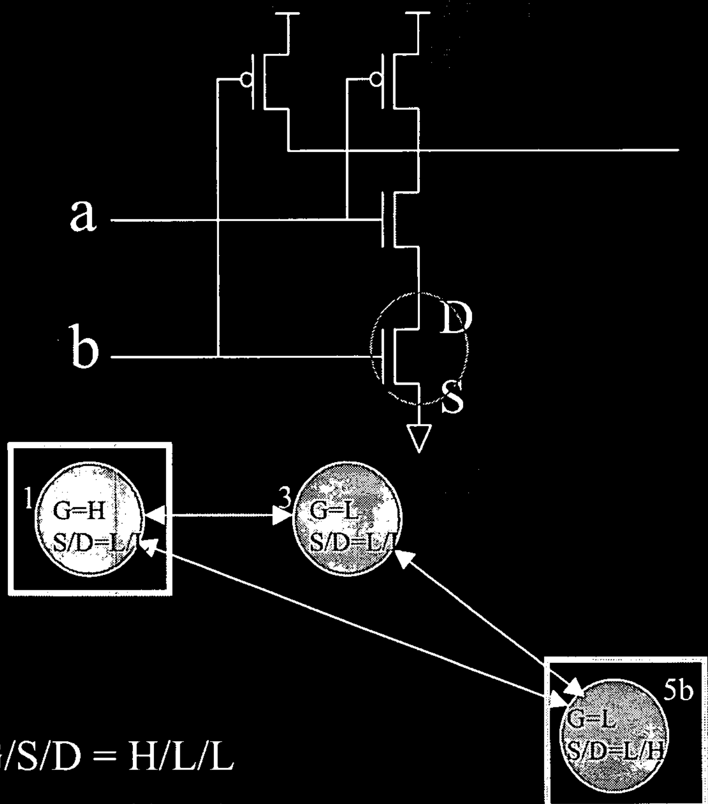
T_{cycle} = 1000 psec

R/F min/max = 400 ps / 600 ps





Monte Carlo results (con't)

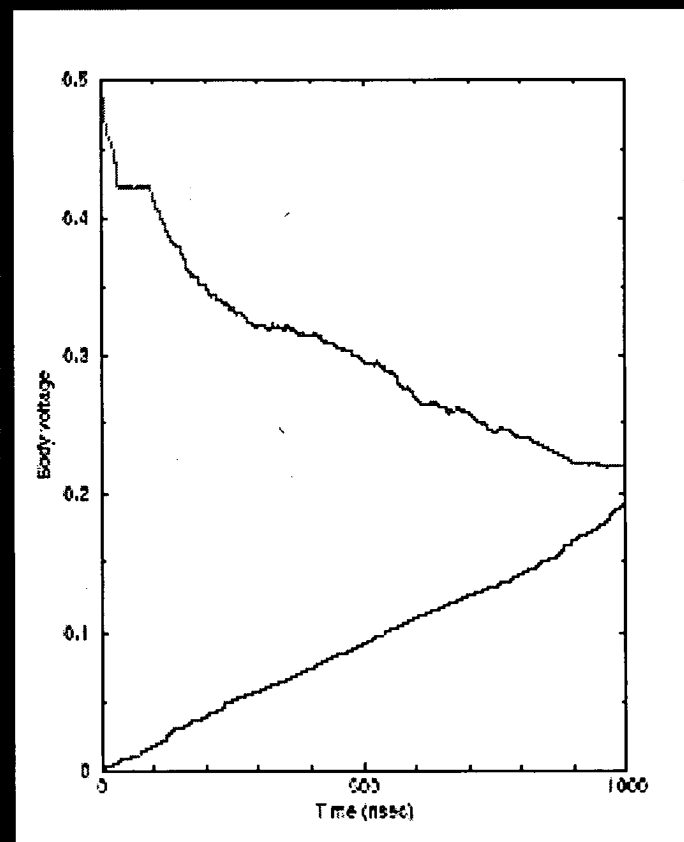


G/S/D = H/L/L

P(a) = P(b) = 0.5

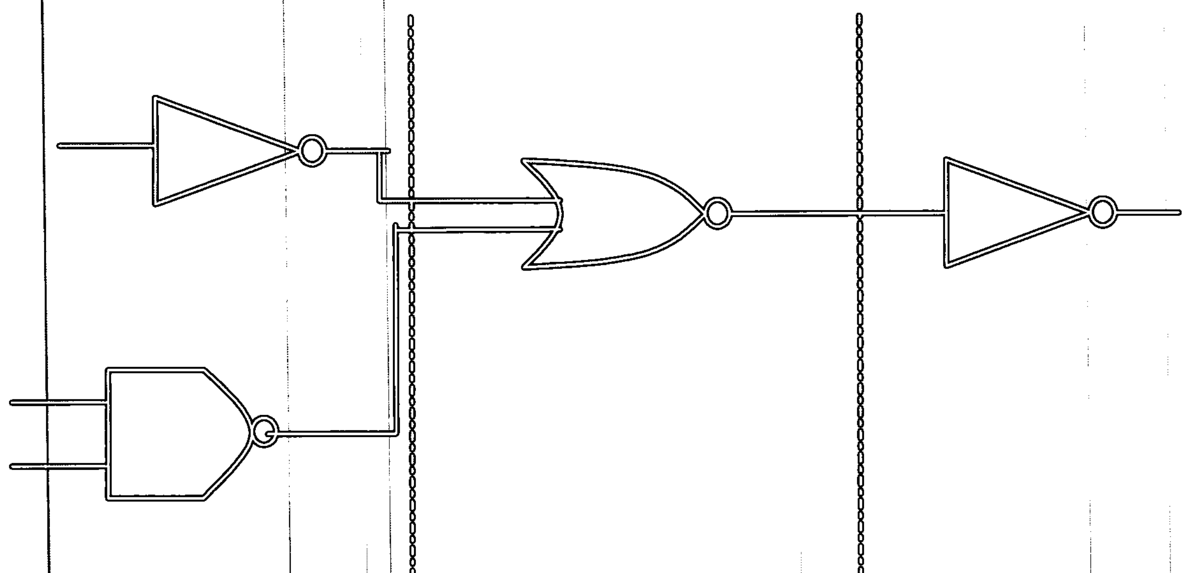
T_{cycle} = 1000 psec

R/F min/max = 400 ps / 600 ps



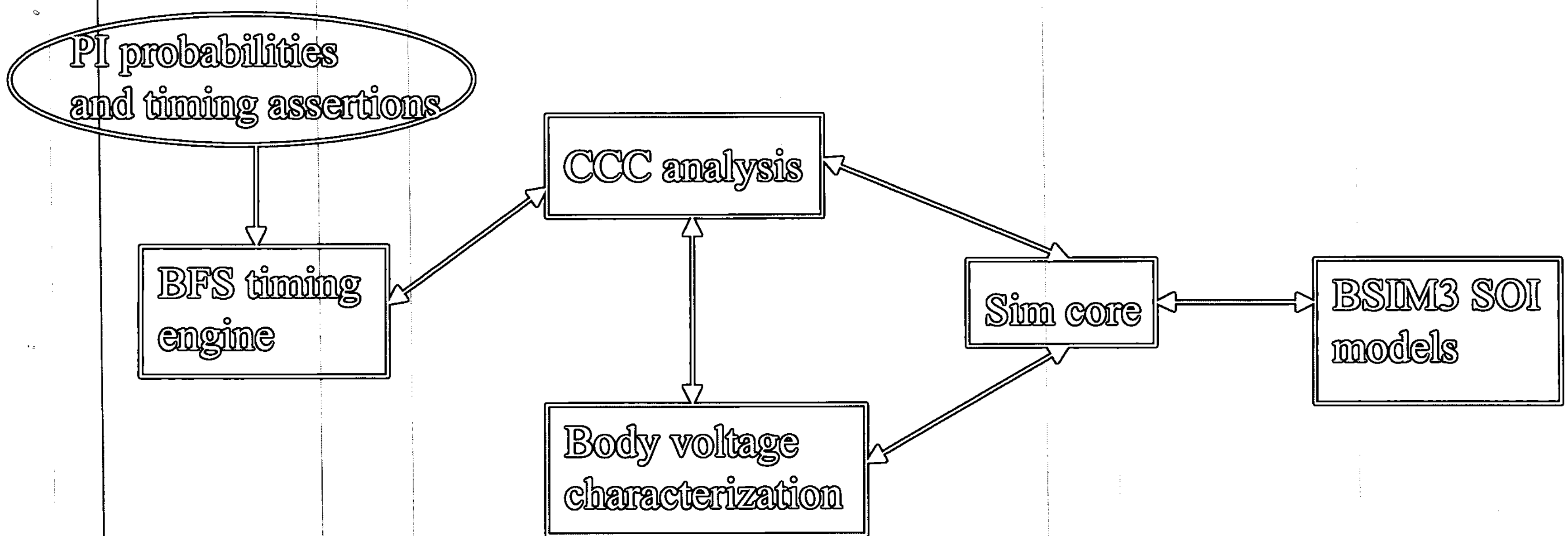
Integrated static timing and body voltage analysis

BFS transistor-level static timing analysis engine



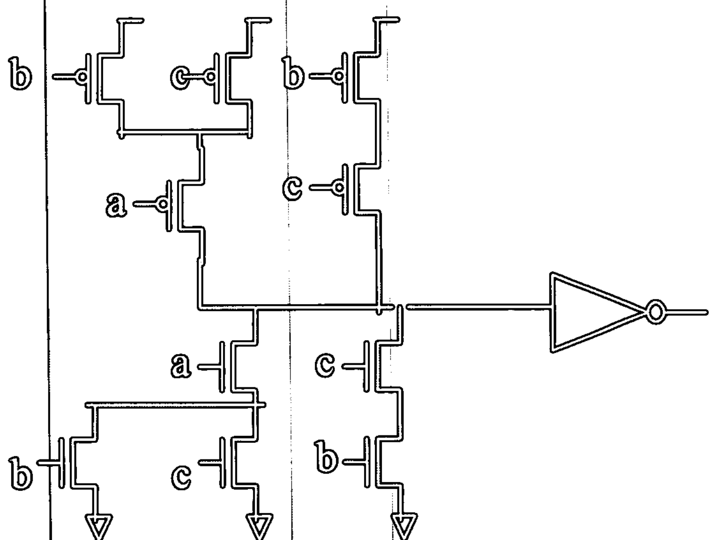
Full PWL waveform propagation
Waveform-delay "morphing"

Architecture of prototype



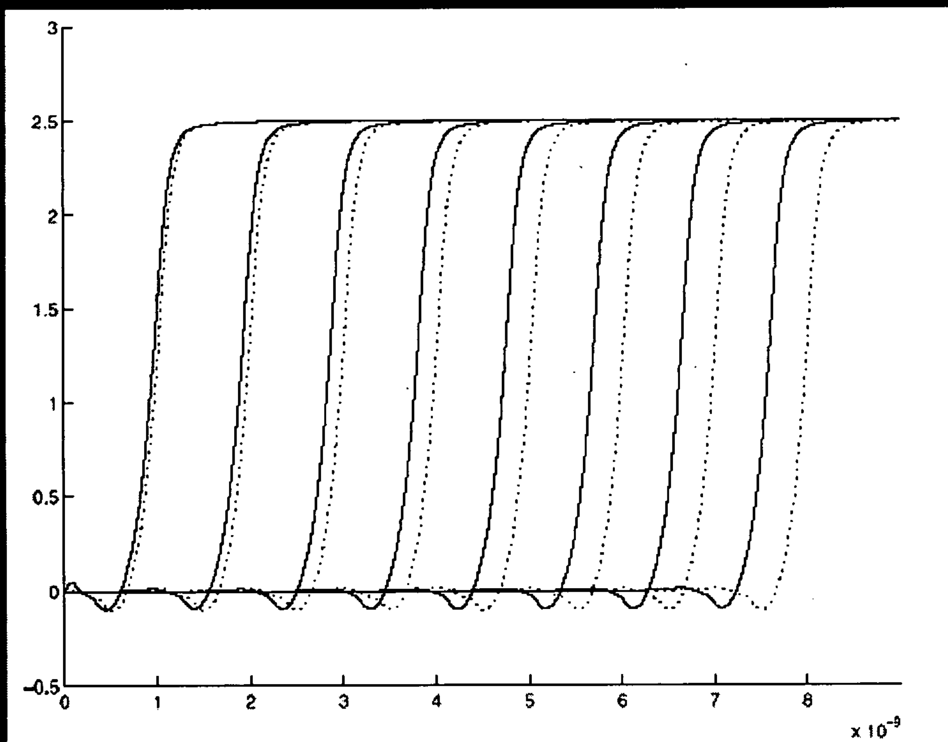
Preliminary timing results

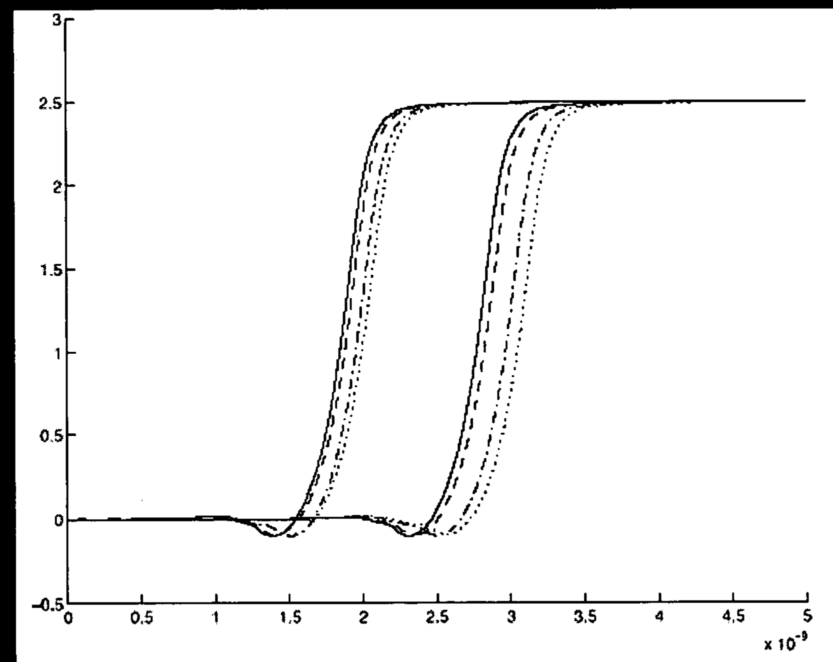
Static ripple-carry adder



16 stages

Preliminary timing results





Stochastic methods for timing and noise?

- Timing tool allows you to immediately identify paths subject to huge "initial condition" delay variability or noise sensitivity that can be reigned in with conservative assumptions of switching activity.
- Body voltages can be applied to static noise analysis
- Integrated timing/noise/body voltage solution required!

Observation: Those circuits that have the most advantage in SOI show the greatest "discrepancy" between initial and steady state results.